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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/574,146	03/29/2006	Guofu Zhou	H-358US	3770

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EXAMINER	
SPAR, ILANA L	

ART UNIT	PAPER NUMBER
2629	

NOTIFICATION DATE	DELIVERY MODE
04/08/2011	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/574,146	ZHOU ET AL.	
	Examiner	Art Unit	
	ILANA SPAR	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 March 2011*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 4-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. Claims 1, 2, 5-7, 9, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Katase (US Patent Publication No. 2002/0021483) in view of Nakamura (US Patent No. 6,628,258).

With reference to claim 1, Katase teaches an electrophoretic display unit comprising

an electrophoretic display panel comprising a plurality of pixels each coupled to a pixel electrode, the plurality of pixels being arranged in a plurality of rows and columns (see paragraph 89, lines 1-6 and 25-26 and Figure 3);

data driving circuitry for supplying a data pulse to each of the pixel electrodes via a switching element associated with each pixel electrode (see paragraph 93);

a common electrode coupled to the plurality of pixels (see paragraph 89, lines 7-8); and

a controller for controlling the data driving circuitry for supplying a setting signal to each of the pixel electrodes for reducing a voltage across the associated pixel (see paragraph 95 and paragraph 140),

wherein the data pulse is supplied during a driving frame period during which each row of pixels is selected in turn (see paragraphs 124-125); and

the setting signal is supplied during a setting frame period (see paragraph 140).

Katase fails to teach that the common electrode receives an alternating voltage signal being reversed in polarity after each setting frame period.

Nakamura teaches an alternating voltage signal applied to the common electrode being reversed in polarity each frame (see column 28, lines 44-46 and line 52-54).

It would have been obvious to one of ordinary skill in the art at the time of invention that the alternating voltage with polarity reversal on the common electrode as taught by Nakamura could be applied to the display as taught by Katase to further improve the image display and reduce the size of the pixel elements (see column 28, line 60 to column 29, line 2), and that, if the voltage alternates once per frame, it would thus alternate after the setting signal is applied, as the setting signal is applied once per frame (i.e. within the frame time, whereas the common voltage alternates as a frame ends). It would further be obvious that Nakamura teaches a reflective active matrix electrooptic display (see column 27, lines 26-29), as is taught in the current invention, and therefore the driving method taught by Nakamura, which enhances the driving transistor, would be applicable to the type of display taught by the current invention.

With reference to claim 2, Katase and Nakamura teach all that is required with reference to claim 1, and Katase further teaches that the switching element comprises a transistor, having a gate, source, and drain, the data driving circuitry being coupled to the source via a data electrode the selection driving circuitry being coupled to the gate via a selection electrode, and the pixel electrode being coupled to the drain (see paragraph 96, lines 5-12).

With reference to claim 5, Katase and Nakamura teach all that is required with reference to claim 1, and Katase further teaches that the setting frame period is shorter

than the driving frame period (see Figure 13, driving frame period Tv and setting frame period Tb).

With reference to claim 6, Katase and Nakamura teach all that is required with reference to claim 1, and Katase further teaches that the alternating voltage signal (common voltage signal) and the setting signal have equal polarities during the setting frame period (see paragraph 140 – the setting signal is used to reduce the voltage across the pixel, such that it would be necessary for the polarity of the signals to be the same in order for the voltage to be reduced).

With reference to claim 7, Katase and Nakamura teach all that is required with reference to claim 1, and Katase further teaches that the amplitude of the alternating voltage signal (common voltage signal) and the amplitude of the setting signal are substantially equal to each other during the setting frame period (see paragraph 140).

With reference to claim 9, Katase and Nakamura teach all that is required with reference to claim 1, and Katase further teaches a storage medium for storing information to be displayed (see paragraph 109).

With reference to claim 10, Katase teaches a method of driving an electrophoretic display panel, which comprises a plurality of pixels each coupled to a pixel electrode, the plurality of pixels being arranged in a plurality of rows and columns, which method comprises the steps of

during a driving frame period during which each row of pixels is selected in turn, supplying a data pulse to each of the pixel electrodes (see paragraph 133);

supplying a voltage signal to a common electrode coupled to the plurality of pixels (see paragraph 133); and

controlling data driving circuitry for supplying, during a setting frame period, a setting signal to each of the pixel electrodes for reducing a voltage across the associated pixel (see paragraph 140).

Katase fails to teach that the common electrode receives an alternating voltage which has a reversal of polarity after each setting frame period.

Nakamura teaches an alternating voltage signal applied to the common electrode being reversed in polarity each frame (see column 28, lines 44-46 and lines 52-54).

It would have been obvious to one of ordinary skill in the art at the time of invention that the alternating voltage with polarity reversal on the common electrode as taught by Nakamura could be applied to the display as taught by Katase to further improve the image display and reduce the size of the pixel elements (see column 28, line 60 to column 29, line 2), and that, if the voltage alternates once per frame, it would thus alternate after the setting signal is applied, as the setting signal is applied once per frame (i.e. within the frame time, whereas the common voltage alternates as a frame ends). It would further be obvious that Nakamura teaches a reflective active matrix electrooptic display (see column 27, lines 26-29), as is taught in the current invention, and therefore the driving method taught by Nakamura, which enhances the driving transistor, would be applicable to the type of display taught by the current invention.

2. Claims 4 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Katase in view of Nakamura as applied to claim 1 above, and further in view of Applicant's Admitted Prior Art.

With reference to claim 4, Katase and Nakamura teach all that is required with reference to claim 1, but fail to teach that the data pulse is supplied during more than one consecutive driving frame period.

Applicant's admitted prior art teaches that the data pulse is supplied during more than one consecutive driving frame period (see page 2, lines 28-30).

It would have been obvious to one of ordinary skill in the art at the time of invention that a data signal may be applied to a display for as many frames as is required in order to properly display the image/video as intended.

With reference to claim 8, Katase and Nakamura teach all that is required with reference to claim 1, but fail to teach the application of a shaking data pulse.

Applicant's admitted prior art teaches that the controller is adapted to control the data driving circuitry to provide any one or more of:

shaking data pulses;

one ore more reset data pulses; and

one or more driving data pulses;

to each pixel (see page 2, lines 22-30).

It would have been obvious to one of ordinary skill in the art at the time of invention that it is advantageous to apply a shaking signal to the display to reduce

display memory of images before writing subsequent images to the display, such that there is less 'sticking' of images, as is common in electrophoretic displays.

Response to Arguments

3. Applicant's arguments filed March 29, 2011 have been fully considered but they are not persuasive. Applicant has argued that the combination of references is inappropriate, as Katase teaches an electrophoretic display, while Nakamura teaches a liquid crystal display. However, Examiner contends that both displays are active matrix electrooptic displays, and the portion of Nakamura is cited to show that the alternating voltage has an effect on the transistor used to drive the pixel, which is the same regardless of which type of active matrix display is being used. Applicant correctly points out that the alternating voltage taught by Nakamura is beneficial in reducing the degradation of the liquid crystal (see Nakamura, column 28, lines 60-64). However, in addition to this benefit, the driving transistors of the active pixel circuit can also be low withstand voltage transistors, which advantageously reduces the size of the pixels and results in a higher definition display (see column 28, line 64 to column 29, line 2). As is well known in the art, an alternating voltage will reduce the voltage swing across a transistor, thus allowing for the lower withstand voltage transistor as taught by Nakamura, and the alternating voltage will further reduce the degradation of the transistor as well as the liquid crystal (see prior art to Ozawa et al., US Patent No. 6,552,315, column 2, lines 18-27). It would therefore be obvious to one of ordinary skill in the art at the time of invention that any active matrix display incorporating transistors would benefit from an alternating voltage in order to reduce degradation of the transistor

element as well as enhancing the definition of the display. As to Applicant's argument that the polarization of light as taught by Nakamura prohibits the combination of Nakamura with Katase, Examiner contends, as above, that enhancing the condition of the pixel, and particularly the transistor, is beneficial regardless of how the display reflects light, and thus Applicant's argument is moot. As to Applicant's further argument that the degradation of a liquid crystal is not applicable to an electrophoretic display, Examiner again points to the above argument that the degradation of the transistor is a separate problem that the use of alternating voltage can correct, which is beneficial to both liquid crystal and electrophoretic displays. Therefore, Examiner disagrees with Applicant's arguments and contends that the combination of Katase and Nakamura is obvious and functional, and results in an improved electrophoretic display of the type taught by the present invention.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ILANA SPAR whose telephone number is (571)270-7537. The examiner can normally be reached on Monday-Thursday 8:00-4:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on (571)272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Bipin Shalwala/
Supervisory Patent Examiner, Art Unit 2629

ILS